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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/945,266	08/31/2001	Richard L. Coulson	42390P11446	3830

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EXAMINER	
CHOI, WOO H	

ART UNIT	PAPER NUMBER
2186	

DATE MAILED: 11/03/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/945,266	COULSON, RICHARD L.	
	Examiner	Art Unit	
	Woo H. Choi	2186	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *31 August 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-46* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-46* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *03/04/02*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Objections

1. Claims 36 and 37 are objected to because of the following informalities:

The dependant claims are written with incomplete sentences, each missing a verb. Appropriate correction is required.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claims 1 – 4, 11 – 13, 18 – 19 and 32 – 34 are rejected under 35 U.S.C. 102(b) as being anticipated by De Martine *et al.* (US Patent No. 5,619,675, hereinafter "De Martine").

4. With respect to claims 1, 11 – 13, 18 – 19 and 32, De Martine discloses a system comprising:

a memory to store data (figure 2, 204) and metadata (figure 3) for the data, the metadata including a plurality of usage bits (302, 304, 306, 308) to indicate usage information for the

memory (abstract), each usage bit corresponding to one of a given number of clock periods (310, 312, 314, 316); and

a memory controller to update the usage bits based on the clock period and to de-allocate the data using the plurality of usage bits (abstract).

5. With respect to claims 2, 3 and 33, the method further comprises:

erasing usage bits corresponding to a new clock period when the new clock period begins (col. 6, lines 51 – 52, see also claim 2).

6. With respect to claims 4 and 34, the method of claim further comprises:

resetting usage bits when an address/tag of the memory is changed (see rejections of claims 2 and 3, usage bits are reset regardless of whether an address/tag is changed, therefore they are resetting when an address/tag of the memory is changed) ; and

setting a usage bit corresponding to a current clock period (see rejection of claim 1, an ICBM that corresponds to a current clock period is set whenever a cache buffer is accessed).

7. Claims 1, 5, 12 – 14, and 32 are rejected under 35 U.S.C. 102(b) as being anticipated by Takamoto *et al.* (US Patent No. 5,606,706, hereinafter "Takamoto").

Takamoto discloses a method (figure 2, 24, col. 4, lines 5 – 8) comprising:

checking a current clock period when a memory is accessed, the current clock period being one of a given number of clock periods (obtaining the reference time requires checking the clock and the number of 'clock periods' or unit of time is finite, or a given number); and

setting a usage bit corresponding to the current clock period (figure 2, 24, each bit contains information regarding the last time the cache segment was used and corresponds to a given number of clock periods or time units), the usage bit indicating usage information for the memory,

wherein the memory is a non-volatile cache memory (figure 1, 6).

8. Claims 1, 5,11 – 14, 18 – 20 and 32, are rejected under 35 U.S.C. 102(e) as being anticipated by Stewart *et al.* (US Patent Publication No. 2003/0005233, hereinafter "Stewart").

With respect to claims Stewart discloses a method (figure 5) comprising:

checking a current clock period when a memory is accessed, the current clock period being one of a given number of clock periods (step 524, time stamping requires checking the clock and the number of 'clock periods' or unit of time is finite, or a given number); and

setting a usage bit corresponding to the current clock period (step 524, each bit of the time stamp contains information regarding when the last cache segment was used and corresponds to a given number of clock periods or time units), the usage bit indicating usage information for the memory,

de-allocating data in the memory based upon the usage bits if the memory is considered full (figure 5),

wherein the memory is a non-volatile cache memory (page 6, paragraph 73).

9. Claims 23 – 25, 35, 36 and 38 – 46 are rejected under 35 U.S.C. 102(e) as being anticipated by Coulson (US Patent No. 6,725,342).

10. With respect to claims 23, 35 and 38, Coulson discloses a method comprising:

storing metadata (figure 5) indicating usage information for a memory; and

updating the metadata during a writeback cycle (figure 6, 635, 640, indication of coherency requires that the dirty bit be reset).

11. With respect to claim 24, the usage information is a least recently used information (col. 5, lines 48 – 50).

12. With respect to claim 25, 36 and 39, storing usage bits as the metadata to indicate the usage information (modified field 504 indicates that the last use of this block of data was write access with modification).

13. With respect to claims 40 and 41, the cache memory is a non-volatile destructive read memory cache memory (col. 4, line 65 – col. 5, line1).

14. With respect to claims 42 – 46, Coulson discloses an apparatus (figure 1) comprising:

a non-volatile destructive read memory (145) to cache data for a storage device and to store usage information (figure 5) for the non-volatile destructive read memory,

a cache controller (140, 150) coupled to the non-volatile destructive read memory; and

a main memory (130) coupled to the cache controller.

wherein the non-volatile destructive read memory is a polymer ferroelectric random access memory (PFRAM), a magnetic RAM (MRAM), or a core memory (col. 4, line 65 – col. 5, line 1),

wherein the storage device (figure 1, 160) is a magnetic or optical memory device.

15. Claims 23 – 26 and 28 are rejected under 35 U.S.C. 102(b) as being anticipated by Hamaguchi (US Patent No. 5,386,546).

16. With respect to claims 23 – 25, Hamaguchi discloses a method comprising:

storing metadata indicating usage information for a memory (figure 1), wherein the usage information is a least recently used information; and

updating the metadata during a writeback cycle (figure 3A, s15, figure 3B, s120 and s140, see also col. 4, lines 7 – 12).

17. With respect to claim 26, updating the metadata comprises:

checking a current clock period (s15, time stamp) when the memory is accessed, the current clock period being one of a predetermined number of clock periods (see rejection of claim 1 based on Takamoto reference above); and

setting a usage bit (s140, new block is loaded with a new time stamp) corresponding to the current clock period, the usage bit indicating usage information for the memory.

18. With respect to claim 28, updating the metadata further comprises:

resetting usage bits (figure 1, old time stamp is erased, i.e. reset, and new time stamp is set, i.e. set again or reset) when an address/tag of the memory is changed (address tag is updated with the address tag of the new block cached); and

setting a usage bit corresponding to a current clock period.

Claim Rejections - 35 USC § 103

19. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

20. Claims 5 – 7, 14, 15, 20 and 21 are rejected under 35 U.S.C. 103(a) as being unpatentable over De Martine in view of Beardsley (US Patent No. 6,502,174, hereinafter "Beardsley").

21. With respect to claims 5, 14 and 20, De Martine discloses all of the limitations of the parent claims as discussed above. However, he does not specifically disclose that the memory is a non-volatile cache memory. On the other hand, Beardsley discloses a system that stores data and metadata where the memory is a non-volatile cache memory (col. 1, lines 60 – 62).

It would have been obvious to one of ordinary skill in the art, having the teachings of De Martine and Bearsley before him at the time the invention was made, to use the non-volatile cache teachings of the storage system with cache of Beardsley in the storage system with cache of De Martine, in order to be able to recover data stored in cache in the event of a power loss (Beardsley, col. 1, lines 57 – 62).

22. With respect to claims 6, 15 and 21, De Martine discloses that the give number of clock cycles is four (figure 3).

23. With respect to claim 7, the difference between De Martine and Beardsley combination and the claim is the value associated with a clock period. However, setting the value of the clock period to a plurality of hours does not have a disclosed purpose nor is it disclosed to overcome any deficiencies in the prior art. Accordingly, it would have been an obvious matter of design choice to set the value of the clock period of the system of De Martine and Beardsley to a plurality of hours, since applicant has not disclosed that setting the clock period to a particular value, overcomes a deficiency in the prior art or is for any stated purpose.

24. Claims 5, 8, 9, 14, 16, 17, 20 and 22 are rejected under 35 U.S.C. 103(a) as being unpatentable over De Martine in view Davis *et al.* (US Patent Application Publication No. 2003/0023922, hereinafter "Davis").

De Martine discloses all of the limitations of the patent claims as discussed above. However, he does not specifically disclose a non-volatile memory that is a destructive read memory. On the other hand, Davis disclose an magnetic RAM that is ideally suited for cache memory (page 6, paragraph 70).

It would have been obvious to one of ordinary skill in the art, having the teachings of De Martine and Davis before him at the time the invention was made, to use the MRAM as cache memory teaching of Davis in the storage system with non-volatile cache memory of De Martine, to take advantage of the low power consumption and relatively fast access speed (Davis, page 3, paragraph 3) while preserving data in the event of a power loss. Davis's MRAM device has an additional advantage of being fault tolerant (page 3, paragraph 5).

25. Claim 27 is rejected under 35 U.S.C. 103(a) as being unpatentable over De Martine in view of Hamaguchi.

De Martine discloses all of the limitations of claim 2, which is substantially the same as claim 27, except for the writeback limitation. De Martine does not specifically disclose that the meta data is updated during a writeback cycle. On the other hand, Hamaguchi discloses a method of updating the metadata during a writeback cycle (see rejection of claim 23 above).

It would have been obvious to one of ordinary skill in the art, having the teachings of De Martine and Hamaguchi before him at the time the invention was made, to use the writeback of

dirty cache teachings of Hamaguchi in the cache system of De Martin, in order to maintain cache coherency as not writing back of dirty data leads to data inconsistency.

26. Claims 10, 29 – 31 are rejected under 35 U.S.C. 103(a) as being unpatentable over De Martine and Hamaguchi in view of Davis.

27. With respect to claims 29 and 31, De Martine and Hamaguchi disclose all of the limitations of the parent claim as discussed above. However, they do not specifically disclose that the memory is a non-volatile cache memory. On the other hand, Davis disclose an magnetic RAM that is ideally suited for cache memory (page 6, paragraph 70).

It would have been obvious to one of ordinary skill in the art, having the teachings of De Martine, Hamaguchi and Davis before him at the time the invention was made, to use the MRAM as cache memory teaching of Davis in the storage system with non-volatile cache memory of De Martine and Hamaguchi, to take advantage of the low power consumption and relatively fast access speed (Davis, page 3, paragraph 3) while preserving data in the event of a power loss. Davis's MRAM device has an additional advantage of being fault tolerant (page 3, paragraph 5).

28. With respect to claim 10, see rejection of claim 27 above.

29. With respect to claims 30, De Martine discloses that the give number of clock cycles is four (figure 3).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Woo H. Choi whose telephone number is (571) 272-4179. The examiner can normally be reached on M-F, 8:00-4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matt Kim can be reached on (571) 272-4182. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

whc
October 28, 2004

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